Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	2	("5239448").PN.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/06/08 18:48
S1	2	("6472735").PN.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/06/02 17:22
S2	134	(dummy near15 align$4) same (frame or chipless)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/06/06 14:27
S3	98	257/686.ccls. and dummy	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/06/06 16:00
S4	67	S3 and @ad<"20020925"	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/06/06 16:05
S5	25	S3 and @rlad<"20020925"	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/06/02 17:31
S6	73	S4 S5	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/06/02 17:31
S7	4	(("6017144") or ("6287935")).PN.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/06/06 14:33

S8	2	("20020153552").PN.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/06/06 14:33
S9	2802	((257/797) or (438/401,462,975)).CCLS.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/06/06 16:05
S10	0	("chipand1").PN.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/06/06 16:05
S11	1167	chip and S9	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/06/06 16:05
S12	987	S11 and @ad<"20020925"	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/06/06 16:05
S13	263	S11 and @rlad<"20020925"	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/06/06 16:05
S14	1040	S12 S13	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/06/06 16:06
S15	447	S14 and bond$3	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/06/07 10:20

S44	6980	(257/686,700,774,777,782).CCLS.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/06/08 13:27
S45	0	("1and@ad<20040324").PN.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/06/08 13:28
S46	6587	S44 and @ad<"20040324"	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/06/08 14:02
S47	1719	S44 and @rlad<"20040324"	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/06/08 13:28
S48	825	stack$4 and S47	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/06/08 13:39
S49	631	top and S48	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/06/08 13:39
S50	41	dummy and S49	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/06/08 13:39
S51	2481	stack$4 and S46	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/06/08 13:39

S52	1721	top and S51	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/06/08 13:39
S53	102	dummy and S52	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/06/08 14:02
S54	0	257/686,685	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/06/08 14:02
S55	2098	(257/685,686).CCLS.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/06/08 14:02
S56	1933	S55 and @ad<"20040324"	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/06/08 14:02
S57	533	S55 and @rlad<"20040324"	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/06/08 14:02
S58	1983	S56 S57	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/06/08 18:47

PATENT ABSTRACTS OF JAPAN

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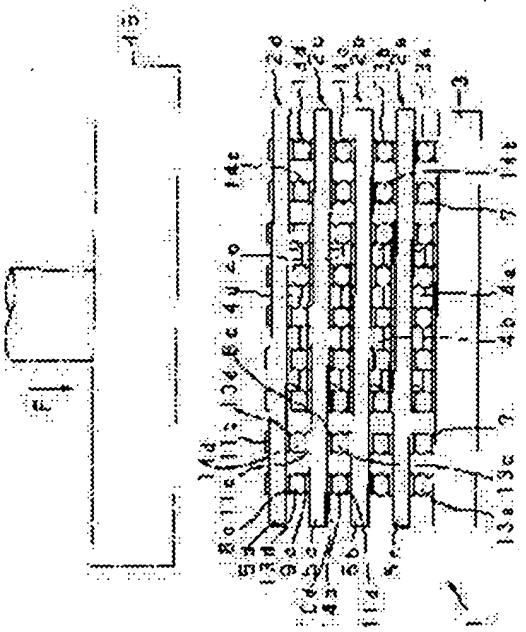
(54) MULTILAYER SEMICONDUCTOR DEVICE AND METHOD OF MANUFACTURING THE SAME

(57)Abstract:

PROBLEM TO BE SOLVED: To improve yield and productivity by high reliability.

SOLUTION: A multiplicity of semiconductor modules each constituted by mounting a semiconductor chip on a wiring board are laminated on a mother board. The respective semiconductor modules are laminated on top of each other or on the mother board via a multiplicity of spacer means provided corresponding to all interlayer connection lands provided on the wiring board of each layer.



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:LAIMS

Claim(s)]
Claim 1] It is the multilayer semiconductor device characterized by to carry out a laminating on mutual and the above-nentioned mother substrate through many spacer means formed in the above-mentioned wiring substrate corresponding o all the interlayer connection lands by which each above-mentioned semi-conductor module was prepared in the wiring ubstrate of each class in the multilayer semiconductor device which comes to carry out the laminating of many semi-onductor modules which mounted the semiconductor chip on the wiring substrate on a mother substrate, respectively.
Claim 2] The above-mentioned spacer means is a multilayer semiconductor device according to claim 1 characterized y being prepared in one wiring substrate of the above-mentioned semi-conductor modules by which a laminating is arried out face to face.
Claim 3] The multilayer semiconductor device according to claim 1 characterized by preparing a dummy land orresponding to the interlayer connection land of the wiring substrate of the semi-conductor module of all each class, nd forming the above-mentioned spacer means in these interlayer connection land and a dummy land with the above-nentioned interlayer connection land which makes connection between the wiring substrates of the above-mentioned emi-conductor module by which a laminating is carried out face to face to the wiring substrate of each above-mentionec emi-conductor module.
Claim 4] The multilayer semiconductor device according to claim 1 characterized by preparing the dummy land orresponding to the number of Maximum connection lands of the semiconductor chip mounted in the wiring substrate f the semi-conductor module of all each class, and forming the above-mentioned spacer means in these connection land nd a dummy land while the connection land of the above-mentioned semiconductor chip mounted separately is preparec n the wiring substrate of each above-mentioned semi-conductor module.
Claim 5] The above-mentioned spacer means is a multilayer semiconductor device according to claim 1 characterized y being a solder ball.
Claim 6] The spacer means formed in the above-mentioned dummy land is a multilayer semiconductor device according o claim 1 characterized by being chosen from metal material, ceramic material, glass material, etc.
Claim 7] In the manufacture approach of the multilayer semiconductor device which comes to carry out the laminating f many semi-conductor modules which mounted the semiconductor chip on the wiring substrate on a mother substrate o each above-mentioned semi-conductor module It has the wiring substrate with which the dummy land corresponding o the interlayer connection land of the wiring substrate of all each class was prepared with the interlayer connection and. The semiconductor chip mounting process of mounting the above-mentioned semiconductor chip in the wiring ubstrate of each above-mentioned semi-conductor module, respectively, The spacer mounting process of attaching a pacer means in the connection land and dummy land of a wiring substrate of each above-mentioned semi-conductor nodule, respectively, The semi-conductor module laminating process which carries out the laminating of each above-nentioned semi-conductor module on mutual and the above-mentioned mother substrate through the above-mentioned pacer means, and by pressing the layered product of each above-mentioned semi-conductor module and the above-nentioned mother substrate The manufacture approach of the multilayer semiconductor device characterized by having he press process unified through the above-mentioned spacer means.
Claim 8] The solder ball supply process which a solder ball is used for the above-mentioned spacer means, and supplies he above-mentioned solder ball to the connection land and dummy land of each above-mentioned wiring substrate ollectively, respectively, Perform 1st heat-treatment to each above-mentioned wiring substrate, and the above-nentioned semi-conductor module is manufactured through the solder ball joining process which carries out melting mmobilization of each above-mentioned solder ball at the above-mentioned connection land and a dummy land. The bove-mentioned semi-conductor module laminating process which carries out the laminating of many above-mentioned emi-conductor modules one by one on the above-mentioned mother substrate, The 2nd heat-treatment a ****** heating rocess and by pressing the layered product of each above-mentioned semi-conductor module and the above-mentioned nother substrate to the layered product of each above-mentioned semi-conductor module and the above-mentioned

nother substrate The manufacture approach of the multilayer semiconductor device according to claim 7 characterized ›y having the press process unified through each above-mentioned solder ball.

Translation done.]

)ETAILED DESCRIPTION

Detailed Description of the Invention]
0001]
Field of the Invention] This invention relates to the multilayer semiconductor device which comes to carry out the aminating of many semi-conductor modules which come to mount a semiconductor chip in a wiring substrate on a nother substrate, and its manufacture approach in more detail about a semiconductor device and its manufacture ıpproach.
0002]
Description of the Prior Art] In the semiconductor device, in order to aim at improvement in the packaging density of a emiconductor chip, the multilayer semiconductor device 100 which comes to carry out the laminating of many semi-:onductor module 101a as shown in drawing 5 thru/or the 101d on the mother substrate 102 is offered. A semiconductor :hip 103 is mounted on flexible INTAPOZA (thin wiring substrate) 104, respectively, and each semi-conductor module .01 is constituted, as shown in drawing 6 (c).
0003] although the mother substrate 102 is a wiring substrate which has mechanical rigidity thicker than the wiring ubstrate 104 of the semi-conductor module 101 and not being illustrated -- a proper connection terminal area and a :ircuit -- a conductor -- the section is formed. Many interlayer connection lands 105 are formed in the mother substrate .02 at the component side of the semi-conductor module 101. By giving polish etc., a semiconductor chip 103 is nounted by anisotropy electric conduction material and soldering 106 grade on the wiring substrate 104, as-izing is :ome [thin shape] and it is shown in drawing 6 (a).
0004] the terminal which connects a semiconductor chip 103 to it although not illustrated in the wiring substrate 104 -- a :onductor -- the section and a proper circuit -- a conductor -- while the section is formed, as shown in drawing 6 (b), nany interlayer connection lands 107 and 108 are formed in the front flesh-side principal plane, respectively. the wiring ubstrate 104 -- each class connection land 107 -- a circuit -- a conductor -- while connecting suitably through the ection, through hole connection was made and this interlayer connection land 107 and the interlayer connection land .08 are suitably connected on the front reverse side. A solder property is given to each class connection lands 107 and .08 by applying flux and soldering paste 109 and 110 to the wiring substrate 104.
0005] The solder ball 111 is supplied to the interlayer connection land 107 required for the wiring substrate 104 in this :ondition. While mounting a semiconductor chip 103, in the condition of having attached the solder ball 111, reflow ıeat-treatment is performed to the wiring substrate 104. Melting immobilization of each solder ball 111 is carried out by his at the interlayer connection land 107, and the wiring substrate 104 manufactures the semi-conductor module 101 by t.
0006] The multilayer semiconductor device 100 consists of 4 lamination which carried out the laminating of the 4th ayer semi-conductor module 101d shown in 1st layer semi-conductor module 101a thru/or this drawing (d) shown in lrawing 7 (a) one by one on the mother substrate 102. It connects with the interlayer connection land 108 to which the nterlayer connection land 107 in which the solder ball 111 is attached so that it may mention later corresponds to 1st ayer semi-conductor module 101a thru/or 4th layer semi-conductor module 101d by through hole connection. Many nterlayer connection lands 107 and 108 which face a front flesh-side principal plane, respectively make a pair in wiring ubstrate 104a thru/or 104d mutually, and are formed in it. In addition, about the interlayer connection lands 107 and .08, the case of explanation where nine pieces are formed in the longitudinal direction is explained for convenience.
0007] 1st layer semi-conductor module 101a is a semi-conductor module directly mounted on the mother substrate 102, ınd as shown in drawing 7 (a), semiconductor chip 103a is mounted in the mother substrate 102 of wiring substrate 104a ınd the principal plane which counters. Solder ball 111a is attached in 1st layer semi-conductor module 101a through oldering paste 109 at all nine interlayer connection land 107a. 2nd layer semi-conductor module 101b is a semi-:onductor module mounted on 1st layer semi-conductor module 101a, and as shown in drawing 7 (b), semiconductor :hip 103b is mounted in 1st layer semi-conductor module 101a of wiring substrate 104b, and the principal plane which

:ounters. Five solder ball 111b is attached in the interlayer connection land 107 in every other one through soldering)aste 109 at 2nd layer semi-conductor module 101b, respectively from left end 1st interlayer connection land 107b.
0008] 3rd layer semi-conductor module 101c is a semi-conductor module mounted on 2nd layer semi-conductor module .01b, and as shown in drawing 7 (c), semiconductor chip 103c is mounted in 2nd layer semi-conductor module 101b of viring substrate 104c, and the principal plane which counters. Four solder ball 111c is attached [from the left end] in he interlayer connection land 107 in every other one through soldering paste 109 at 3rd layer semi-conductor module .01c, respectively from 2nd interlayer connection land 107c.
0009] 4th layer semi-conductor module 101d, it is the semi-conductor module mounted on 3rd layer semi-conductor nodule 101c, and as shown in drawing 7 (d), 103d of semiconductor chips is mounted in 3rd layer semi-conductor nodule of 104d of wiring substrates 101c, and the principal plane which counters. Five solder ball 111c is attached like / 4th layer semi-conductor module 101d / 2nd layer semi-conductor module 101b] in the interlayer connection and 107 in every other one through soldering paste 109, respectively from left end 1st interlayer connection land 107c.
0010] 1st layer semi-conductor module 101a makes a semiconductor chip component side counter to the mother ubstrate 102 through a proper positioning device, and a laminating is carried out, and it is joined to the interlayer :onnection land 105 to which each solder ball 111a corresponds through soldering paste 110. 2nd layer semi-conductor nodule 101b makes a semiconductor chip component side counter to 1st layer semi-conductor module 101a, a aminating is carried out, and temporary junction is carried out through interlayer connection land 108a and soldering)aste 110 with which each solder ball 111b corresponds. Hereafter, the laminating of 3rd layer semi-conductor module .01c and the 4th layer semi-conductor module 101d is carried out one by one similarly.
0011] While reflow heat-treatment is performed and making each solder ball 111 between each class into a melting :ondition, as the drawing 5 chain line shows, press processing is performed to the mother substrate 102 and 1st layer emi-conductor module 101a thru/or a 4th layer semi-conductor module 101d layered product by the push plate 112 from he 1st layer semi-conductor module 101a side. It is fixed to the interlayer connection land 108 to which each solder ball .11 corresponds, mechanical association and predetermined electrical installation are performed, and the mother ubstrate 102 and 1st layer semi-conductor module 101a thru/or a 4th layer semi-conductor module 101d layered produc :onstitute the multilayer semiconductor device 100.
0012]
Problem(s) to be Solved by the Invention] The solder ball 111 is attached only in the part corresponding to the part vhich should perform electrical installation between each class as mentioned above in the conventional multilayer emiconductor device 100. Therefore, in the multilayer semiconductor device 100, as shown in drawing 5 , the space ection h1 of a large number to which the solder ball 111 does not exist in the bottom, respectively between 1st layer emi-conductor module 101a thru/or 4th layer semi-conductor module 101d each class thru/or h3 are constituted.
0013] while the thin wiring substrate 104 is used for the semi-conductor module 101, respectively and the interlayer :onnection lands 107 and 108 are also miniaturized by the multilayer semiconductor device 100 -- a circuit -- a :onductor -- the section is also formed into the ** pitch. In the multilayer semiconductor device 100, as mentioned bove, after carrying out the laminating of each part material, press processing by the push plate 112 is performed, but in)rder that there may be no support by the solder ball 111 in each space section h, it will be in the condition that the viring substrate 104 bends and thrust does not get across to the bottom.
0014] For this reason, in the multilayer semiconductor device 100, each solder ball 111, flux, and the interlayer :onnection lands 107 and 108 were not connected certainly, but while dependability deteriorated, there was a problem hat the yield was bad. The multilayer semiconductor device 100 becomes much more remarkable [this problem] as it)ecomes a multilayer. Moreover, in the multilayer semiconductor device 100, since a faulty connection's part was generated in a inner layer, flow inspection of the total which used flow test equipment needed to be carried out, and there vas a problem that productive efficiency was bad. Furthermore, in the multilayer semiconductor device 100, since the hin wiring substrate 104 was used, there was a problem that handling was troublesome. Since a number of each solder)all 111 which is different to the semi-conductor module 101 of each class, respectively was attached in the multilayer emiconductor device 100 further again, respectively, there was a problem that setting out of a feeder was troublesome.
0015] Therefore, this invention solves the conventional trouble mentioned above, is reliable and is proposed for the)urpose of offering the multilayer semiconductor device with which improvement in the yield or productivity was chieved, and its manufacture approach.
0016]
Means for Solving the Problem] The multilayer semiconductor device concerning this invention which attains the objec nentioned above comes to carry out the laminating of many semi-conductor modules which mounted the semiconductor :hip on the wiring substrate on a mother substrate. many spacer means formed in the wiring substrate corresponding to ll the interlayer connection lands by which each semi-conductor module was prepared in the wiring substrate of each :lass, respectively -- minding -- mutual -- or a laminating is carried out on a mother substrate.

0017] According to the multilayer semiconductor device concerning this invention constituted as mentioned above, ince thrust is transmitted to homogeneity to the semi-conductor module of each class through many spacer means, onnection of an interlayer connection land is made certainly and simply. According to the multilayer semiconductor levice, since many spacer means are attached to a thin wiring substrate, while each mechanical rigidity also improves, he handling at the time of a laminating process also becomes simple. According to the multilayer semiconductor device, nstallation of a spacer means is performed using a common feeder to the semi-conductor module of each class.
0018] Moreover, as for the manufacture approach of the multilayer semiconductor device concerning this invention vhich attains the object mentioned above, the wiring substrate with which the dummy land corresponding to the nterlayer connection land of the wiring substrate of all each class in an interlayer connection land was prepared is used it each semi-conductor module. The semiconductor chip mounting process that the manufacture approach of a multilaye emiconductor device mounts a semiconductor chip in the wiring substrate of each semi-conductor module, respectively, The spacer mounting process of attaching a spacer means in the connection land and dummy land of a wiring substrate o ach semi-conductor module, respectively, It has the semi-conductor module laminating process which carries out the aminating of each semi-conductor module on mutual and a mother substrate through a spacer means, and the press rocess which unifies each part material through a spacer means by pressing the layered product of each semi-conductor nodule and a mother substrate.
0019] According to the manufacture approach of the multilayer semiconductor device concerning this invention which as the above process, since thrust is transmitted to homogeneity to the semi-conductor module of each class through nany spacer means, connection of an interlayer connection land comes to be made certainly and simply. According to he manufacture approach of a multilayer semiconductor device, since many spacer means are attached in homogeneity o a thin wiring substrate, respectively, while each mechanical rigidity also improves, the handling at the time of carrying ut the laminating of each part material is performed simple. According to the manufacture approach of a multilayer emiconductor device, installation of a spacer means is performed using a common feeder to the semi-conductor module f each class, and simplification of a process is attained.
0020]
Embodiment of the Invention] Hereafter, the gestalt of operation of this invention is explained to a detail with reference o a drawing. The multilayer semiconductor device 1 shown as a gestalt of operation makes almost the same the onventional multilayer semiconductor device 100 mentioned above and a fundamental configuration, and as shown in lrawing 1 , the laminating of many semi-conductor module 2a thru/or the 2d is carried out on the mother substrate 3, and t becomes. A semiconductor chip 4 is mounted on the thin wiring substrate 5, respectively, and each semi-conductor nodule 2 is constituted, as shown in drawing 2 (c). Although the multilayer semiconductor device 1 is not illustrated, it nay be made to **** between each class with insulating resin.
0021] semiconductor chips 2 being chip objects, such as an integrated circuit device and a memory chip, and giving olish etc. -- a thin shape ---izing is come As shown in drawing 2 (a), connection mounting of the semiconductor chip 2 s carried out by anisotropy electric conduction material and soldering 6 grade on the mounting field of the wiring ubstrate 5. A semiconductor chip 2 may be made to carry out connection mounting on the wiring substrate 5 by virebonding.
0022] although the mother substrate 3 is not illustrated while the wiring substrate which has mechanical rigidity by big hickness is used and it constitutes the base of the multilayer semiconductor device 1 from a wiring substrate 5 of the emi-conductor module 2 -- copper foil etc. -- a proper connection terminal area and a circuit -- a conductor -- the sectior s formed and external connection material is constituted. Many interlayer connection lands 7 are formed in the mother ubstrate 3 at the component side of the semi-conductor module 2. the interlayer connection land 7 -- a circuit -- a onductor -- while connecting with the section, a connection terminal with the semi-conductor module 2 by which a aminating is carried out is constituted.
0023] although the wiring substrate 5 uses for example, an insulating film as a base material and a detail is omitted to he principal plane -- copper foil etc. -- a proper circuit -- a conductor -- while the section is formed -- the mounting field f a semiconductor chip 2 -- surrounding -- a terminal -- a conductor -- the section is formed. Many interlayer connectior ands 8 and 9 and dummy lands 10 and 11 are formed in the wiring substrate 5 at the front flesh-side principal plane. In ddition, the wiring substrate 5 not only mounts a semiconductor chip 2 directly on a principal plane, but may clip and orm the hole which a semiconductor chip 2 is made to face, or you may make it form the perforation for performing ontinuation conveyance along with edges on both sides etc.
0024] while making a pair to the front flesh-side principal plane of the wiring substrate 5, respectively, forming them in t, although each class connection lands 8 and 9 omit a detail, and connecting mutually by through hole connection -- a ircuit -- a conductor -- it is the land connected with the section. although each dummy lands 10 and 11 omit a detail -- he table rear face of the wiring substrate 5 -- setting -- respectively -- a circuit -- a conductor -- it is the land which ecame independent on the independent land or the front flesh side by which through hole connection is not made which

s not connected with the section.
0025] It comes almost uniformly to carry out distribution formation of many lands which make a pair to a front flesh-ide principal plane, respectively at the wiring substrate 5 by carrying out for example, a matrix-like array etc. Each land :onstitutes the interlayer connection lands 8 and 9 and the dummy lands 10 and 11 by making suitably each connection vhich mentioned the wiring substrate 5 above corresponding to the semi-conductor module 2 of each class. The dummy ands 10 and 11 are formed in the location where these interlayer connection lands 8 and 9 are not formed in the wiring ubstrate 5 concerned corresponding to all the interlayer connection lands 8 and 9 formed in the wiring substrate 5 of :ach class at least, respectively. in addition, the dummy lands 10 and 11 -- the magnitude of the wiring substrate 5, hickness, the rate of elastic deformation, or a circuit -- a conductor -- according to the pitch of the section etc., you may orm suitably in common with each wiring substrate 5 irrespective of the existence of the interlayer connection lands 8 nd 9.
0026] As shown in drawing 2 (b), a solder property is given to the wiring substrate 5 by applying flux and soldering aste 12 to the interlayer connection lands 8 and 9 or the dummy lands 10 and 11. Where soldering paste 12 grade is pplied to the wiring substrate 5, all the interlayer connection lands 8 and dummy lands 10 by the side of the component ide of a semiconductor chip 4 are collectively supplied by the feeder which the solder ball 13 for connection and the older ball 14 for dummy connection do not illustrate. In addition, each solder ball 13 for connection and the solder ball .4 for dummy connection are altogether the same.
0027] While a semiconductor chip 4 is mounted, in the condition of having attached the solder ball 13 for connection, nd the solder ball 14 for dummy connection in the interlayer connection land 8 or the dummy land 10, reflow heat-reatment is performed to the wiring substrate 5. Melting immobilization of each solder ball 13 for connection or the older ball 14 for dummy connection is carried out by this processing at the interlayer connection land 8 and the dummy and 10, respectively, and the wiring substrate 5 manufactures the semi-conductor module 2 shown in drawing 2 (c) by it

0028] Although the semi-conductor module 2 uses the thin wiring substrate 5 as a base material as mentioned above, it as the structure where mechanical rigidity is large by carrying out junction immobilization, and weight balance was alsc djusted for the solder ball 13 for connection, or the solder ball 14 for dummy connection by homogeneity. Therefore, vhile the handling in the production process later mentioned by this of the semi-conductor module 2 becomes easy, generating of the inconvenience that a faulty connection arises in the semiconductor chip 4 mounted according to leformation etc. comes to be controlled.
0029] The multilayer semiconductor device 1 consists of 4 lamination which carried out the laminating of the 4th layer emi-conductor module 2d shown in 1st layer semi-conductor module 2a thru/or this drawing (d) shown in drawing 3 (a) ne by one on the mother substrate 3. 1st layer semi-conductor module 2a thru/or 4th layer semi-conductor module 2d, he interlayer connection lands 8 and 9 and the dummy lands 10 and 11 which the interlayer connection lands 8 and 9 :onnected suitably are formed as mentioned above, and serve as the same number on the whole are formed. In addition, lthough nine interlayer connection lands 8 and 9 and dummy lands 10 and 11 are illustrated on the whole by 1st layer emi-conductor module 2a thru/or 4th layer semi-conductor module 2d at the table rear face, of course, much these are ctually arranged for example, in the shape of a matrix.
0030] 1st layer semi-conductor module 2a is a semi-conductor module directly mounted on the mother substrate 3, and s shown in this drawing (a), semiconductor chip 4a is mounted in the mother substrate 3 of wiring substrate 5a, and the rincipal plane five a1 which counters. All nine by which 1st layer semi-conductor module 2a is formed in a principal lane five a1 lands are interlayer connection land 8a, and joining immobilization of the solder ball 13a for connection is arried out on these interlayer connection land 8a, respectively. Nine lands by which 1st layer semi-conductor module 2a s formed in the another side principal plane five a2 set a left end to interlayer connection land 9a, and interlayer :onnection land 9a and dummy land 11a are constituted by turns.
0031] 2nd layer semi-conductor module 2b is a semi-conductor module mounted on 1st layer semi-conductor module !a, and as shown in drawing 3 (b), semiconductor chip 4b is mounted in the opposed face five b1 with 1st layer semi-:onductor module 2a of wiring substrate 5b. 2nd layer semi-conductor module 2b sets a left end to interlayer connection and 8b corresponding to nine land configurations by the side of the principal plane five a2 of 1st layer semi-conductor nodule 2a which nine lands formed in the principal plane five b1 of wiring substrate 5b mentioned above, and interlayer :onnection land 8b and dummy land 10b are constituted by turns. While joining immobilization of the solder ball 13b fo :onnection is carried out at 2nd layer semi-conductor module 2b at each class connection land 8b, respectively, joining mmobilization of the solder ball 14b for dummy connection is carried out at each dummy land 10b, respectively. Nine ands by which 2nd layer semi-conductor module 2b is formed in the another side principal plane five b2 set a left end to lummy land 11b, and dummy land 11b and interlayer connection land 9b are constituted by turns.
0032] 3rd layer semi-conductor module 2c is a semi-conductor module mounted on 2nd layer semi-conductor module !b, and as shown in drawing 3 (c), semiconductor chip 4c is mounted in the opposed face 5c1 with 2nd layer semi-

:onductor module 2b of wiring substrate 5c. 3rd layer semi-conductor module 2c sets a left end to dummy land 10c :orresponding to nine land configurations by the side of the principal plane five b2 of 2nd layer semi-conductor module !b which nine lands formed in the principal plane 5c1 of wiring substrate 5c mentioned above, and dummy land 10c and nterlayer connection land 8c are constituted by turns. While joining immobilization of the solder ball 13c for connection s carried out at 3rd layer semi-conductor module 2c at each class connection land 8c, respectively, joining mmobilization of the solder ball 14c for dummy connection is carried out at each dummy land 10c, respectively. Nine ands by which 3rd layer semi-conductor module 2c is formed in the another side principal plane 5c2 set a left end to nterlayer connection land 9c, and interlayer connection land 9c and dummy land 11c are constituted by turns.

0033] 4th layer semi-conductor module 2d, it is the semi-conductor module mounted on 3rd layer semi-conductor nodule 2c, and as shown in drawing 3 (d), 4d of semiconductor chips is mounted in 1 5d of opposed faces with 3rd layer ,emi-conductor module 2c of 5d of wiring substrates. 4th layer semi-conductor module 2d, nine lands formed in 1 5d of)rincipal planes of 5d of wiring substrates set a left end to interlayer connection land 8d corresponding to nine land :onfigurations by the side of the principal plane 5c2 of 3rd layer semi-conductor module 2c mentioned above, and nterlayer connection land 8d and dummy land 10d are constituted by turns. 4th layer semi-conductor module 2d -- each :lass connection land 8cd -- while joining immobilization of the solder ball 13d for connection is carried out, espectively, joining immobilization of the solder ball 14d for dummy connection is carried out at each dummy land 10d, espectively. 4th layer semi-conductor module 2d, 2 constitutes the surface of the multilayer semiconductor device 1 5d)f principal planes of another side.

0034] Next, with reference to drawing 4 , the production process of the multilayer semiconductor device 1 is explained. \fter manufacturing the semi-conductor module 2 of each class, the multilayer semiconductor device 1 carries out the aminating of these semi-conductors module 2 on the mother substrate 3, unifies and is manufactured. A production)rocess mounts a semiconductor chip 4 in the mounting field of the wiring substrate 5 for the semiconductor chip nounting process s-1 by anisotropy electric conduction material or soldering 6 grade as the 1st process. In a production)rocess, processing which applies flux and soldering paste to the interlayer connection lands 8 and 9 and the dummy ands 10 and 11 which were formed in each wiring substrate 5, and gives the junction property and soldering nature of he solder balls 13 and 14 is performed in the soldering nature grant process s-2.

0035] In the solder ball supply process s-3, to the interlayer connection land 8 and the dummy land 10 by the side of the ,emiconductor chip component side of the wiring substrate 5, the solder ball 13 for connection and the solder ball 14 for lummy connection are put in block by the feeder, and it supplies in a production process. Temporary junction of the ,older ball 13 for connection and the solder ball 14 for dummy connection is carried out with soldering paste etc. at the nterlayer connection land 8 and the dummy land 10.

0036] In a production process, junction immobilization of the solder ball 13 for connection or the solder ball 14 for lummy connection is carried out in the solder ball joining process s-4 at the interlayer connection land 8 and the dummy and 10 which fuse and correspond, respectively by throwing the wiring substrate 5 into a reflow solder tub, and)erforming 1st heat-treatment. In a production process, the semi-conductor module 2 is manufactured through the above)rocess.

0037] In a production process, processing which applies flux and soldering paste to the front face of the interlayer :onnection land 9 formed in the principal plane of another side of the manufactured semi-conductor module 2, the lummy land 11 or the solder ball 13 for connection by which junction immobilization was carried out, or the solder ball .4 for dummy connection, and gives soldering nature is performed in the soldering nature grant process s-5.

0038] In a production process, the laminating of semi-conductor module 2a of a predetermined number thru/or the 2d is :arried out one by one to the mother substrate 3 in the semi-conductor module laminating process s-6. Flux and soldering)aste are applied to the interlayer connection land 7, and soldering nature is also given to the mother substrate 3. Through flux or soldering paste, mutually, temporary maintenance of the laminating condition is carried out, and it :onstitutes class semi-conductor module 2a thru/or 2d of layered products with the mother substrate 3.

0039] In a production process, in the heating process s-7, the mother substrate 3, class semi-conductor module 2a, or a !d layered product is supplied to a reflow solder tub, and 2nd heat-treatment is performed. Class semi-conductor module !a thru/or the 2d solder ball 13 for connection, and the solder ball 14 for dummy connection fuse a layered product, espectively, and junction immobilization is carried out at the interlayer connection land 9 and the dummy land 10 which :ounter, respectively.

0040] In a production process, press processing by the push plate 15 shown with the drawing 1 chain line from the 4th ayer semi-conductor module 2d side is performed in the press process s-8. Connection immobilization of the interlayer :onnection land 7 of the mother substrate 3, class semi-conductor module 2a thru/or the 2d interlayer connection lands 8 ınd 9 or the dummy lands 10 and 11, and the solder ball 13 for connection of each class and the solder ball 14 for lummy connection is firmly carried out by this press processing, and a production process completes the multilayer ,emiconductor device 1.

0041] The multilayer semiconductor device 1 is arranged in the condition with uniform solder ball 13 for connection ınd solder ball 14 for dummy connection between the mother substrate 3, class semi-conductor module 2a, or 2d, as nentioned above. If it puts in another way, the multilayer semiconductor device 1 has structure which class semi-:onductor module 2a thru/or the 2d interlayer connection lands 8 and 9 supported altogether with the solder ball 13 for :onnection, or the solder ball 14 for dummy connection as shown in drawing 1 .
0042] Therefore, positive connection is made by the thrust F according [the multilayer semiconductor device 1] to a)ush plate 15 being transmitted to class semi-conductor module 2a thru/or all the 2d interlayer connection lands 8 and 9 hrough the solder ball 13 for these connection, and the solder ball 14 for dummy connection. While handling becomes :asy since the multilayer semiconductor device 1 has large mechanical rigidity by carrying out class semi-conductor nodule 2a thru/or 2d at the wiring substrate 5, and carrying out junction immobilization of the solder ball 13 for :onnection, or the solder ball 14 for dummy connection at homogeneity and has an as a whole still bigger mechanical .trength, generating of the faulty connection of the semiconductor chip 4 by deformation of the wiring substrate 5 etc. is :ontrolled.
0043] In the multilayer semiconductor device 1 mentioned above, although the dummy lands 10 and 11 were formed in he front flesh-side principal plane of the wiring substrate 5 which constitutes the semi-conductor module 2 with the nterlayer connection lands 8 and 9, the dummy lands 10 and 11 may be formed only in any or one side. As for the viring substrate 5, the number of lands is reduced by this configuration.
0044] Moreover, in the multilayer semiconductor device 1, although it constituted so that the interlayer connection land: 3 and 9 might be supported with the solder ball 14 for dummy connection, the spacer formed, for example with metal :hips, such as brass and stainless steel, ceramic chips, such as an alumina, a glass chip, etc. may be used. By applying lux etc., soldering nature is given and connection immobilization of the spacer is carried out at a wiring substrate.
0045]
Effect of the Invention] As explained to the detail above, according to the multilayer semiconductor device concerning his invention, and its manufacture approach many spacer means by which each semi-conductor module was prepared in he wiring substrate of each class corresponding to all the interlayer connection lands prepared, respectively -- minding -- nutual -- or from a laminating being carried out on a mother substrate Thrust is transmitted to homogeneity to the semi-:onductor module of each class through a spacer means, connection of an interlayer connection land is made certainly ınd simply, and improvement in dependability and the yield is achieved. According to the multilayer semiconductor levice, improvement in productivity is achieved by making simple the handling at the time of a laminating process, :ontrolling generating of the faulty connection of the semiconductor chip by the browning form, while each mechanical igidity also improves, since many spacer means are attached to a thin wiring substrate, and enabling installation of a ,pacer means using a common feeder to the semi-conductor module of each class.

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Translation

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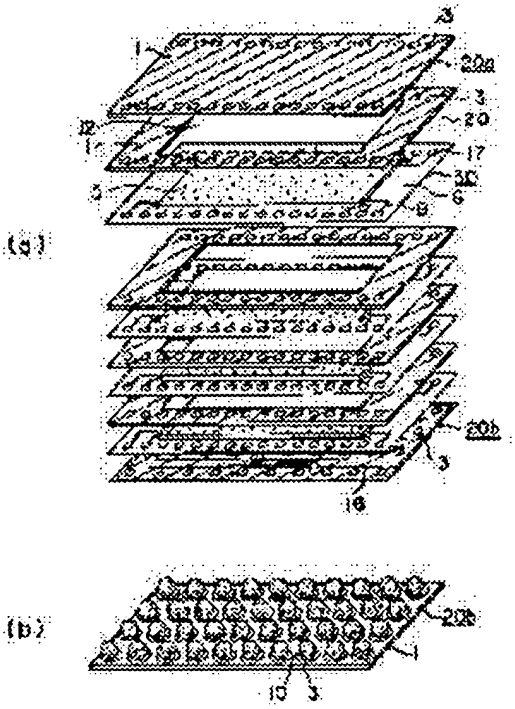
(54) SEMICONDUCTOR DEVICE AND ITS MANUFACTURE

(57)Abstract:

PROBLEM TO BE SOLVED: To obtain a semiconductor device using a laminated package which is thin and has superior hermetical property and resiliency and can be manufactured easily through a simple manufacturing process, and a method for manufacturing the device.

SOLUTION: A semiconductor device has a plurality of wiring boards 30 each of which is provided with a plurality of via holes in which connecting electrodes are formed under lands 17 and wiring 8 electrically connected to the connecting electrodes, semiconductor elements 5 which are mounted on the wiring boards 30 and electrically connected to the wiring 8, and chip cavity sections 12 in which the semiconductor elements 5 are housed when the elements 5 are mounted on the boards 30. The semiconductor device is also provide with a plurality of conductive via-hole insulating substrates 20 provided with connecting electrodes which are buried in the via holes and formed under the lands 3. The thicknesses of the semiconductor elements 5 are adjusted to about 30-200 μm. Therefore, a semiconductor device having a thin laminated package can be obtained. Even when the semiconductor elements 5 elongate a little, the elongation of the elements 5 can be absorbed by the spaces formed between the elements 5 and chip cavity sections 12 when the semiconductor device is bent.



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CLAIMS

Claim(s)]

Claim 1] Two or more wiring substrates equipped with wiring electrically connected to two or more beer with which the connection electrode was formed, respectively, and this connection electrode, The semiconductor device which was carried in said wiring substrate and connected to said wiring and electric target, It has the larger chip cavity section than the semiconductor device volume in which this semiconductor device is held when said semiconductor device is carried. Two or more electric conduction beer insulating substrates equipped with the connection electrode which embedded from two or more beer and was formed are provided. One of said the electric conduction beer insulating substrates and one of said the wiring substrates A laminating is carried out and a layered product is constituted so that said connection wiring of said electric conduction beer insulating substrate and said connection electrode of this wiring substrate may be electrically connected to said wiring substrate. It is the semiconductor device characterized by the laminating of two or more these layered products being carried out, and coming to unify them where said semiconductor device carried in said wiring substrate is thoroughly held in said chip cavity section.

Claim 2] Two or more wiring substrates equipped with wiring electrically connected to two or more beer with which the connection electrode was formed, respectively, and this connection electrode, The semiconductor device which was carried in said wiring substrate and connected to said wiring and electric target, Two or more electric conduction beer insulating substrates equipped with the connection electrode which has the larger chip cavity section than the semiconductor device volume in which this semiconductor device is held when said semiconductor device is carried, embedded from two or more beer, and was formed, When the laminating of said wiring substrate and the electric conduction beer insulating substrate is carried out, a laminating is carried out on the electric conduction beer insulating substrate of the maximum upper layer. The electric conduction beer insulating substrate of the upper layer equipped with the connection electrode which embedded from two or more beer and was formed is provided. One of said the electric conduction beer insulating substrates and one of said the wiring substrates A laminating is carried out and a layered product is constituted so that said connection wiring of said electric conduction beer insulating substrate and said connection electrode of this wiring substrate may be electrically connected to said wiring substrate. It is the semiconductor device characterized by the laminating of two or more these layered products being carried out where said semiconductor device carried in said wiring substrate is thoroughly held in said chip cavity section, and coming to be unified.

Claim 3] Said semiconductor device is a semiconductor device according to claim 1 or 2 characterized by the thickness being abbreviation 30 thru/or 200 micrometers.

Claim 4] The laminating of said two or more layered products by which the laminating was carried out is carried out, and the lower layer electric conduction beer insulating substrate equipped with the connection electrode which embedded from two or more beer and was formed is provided. The wiring substrate of the lowest layer of said layered product is contacted in said 1st lower layer field of an electric conduction beer insulating substrate. Said connection electrode of the wiring substrate of said lowest layer and said connection electrode of said lower layer electric conduction beer insulating substrate are connected electrically. The semiconductor device according to claim 1 to 3 characterized by forming two or more external terminals electrically connected to said 2nd lower layer page through the connection electrode and wiring which were formed in said beer.

Claim 5] The semiconductor device according to claim 1 to 4 characterized by forming the space which absorbs stress between said semiconductor devices contained by said chip cavity section and this chip cavity section of said electric conduction beer insulating substrate.

Claim 6] The semiconductor device according to claim 4 characterized by filling up said space with elasticity adhesives

Claim 7] The process which forms two or more wiring substrates equipped with wiring electrically connected to two or more beer with which the connection electrode was formed, respectively, and this connection electrode, The process which makes the semiconductor device electrically connected with said wiring carry in said wiring substrate, and when

aid semiconductor device is carried The process which forms two or more electric conduction beer insulating substrates vhich have the larger chip cavity section than the semiconductor device volume in which this semiconductor device is ıeld, and were equipped with the connection electrode which embedded from two or more beer and was formed, and ormed the adhesives layer in the rear face, One of said the electric conduction beer insulating substrates and one of said he wiring substrates A laminating is carried out so that said connection wiring of said electric conduction beer insulating ubstrate and said connection electrode of this wiring substrate may be electrically connected to said wiring substrate. The manufacture approach of the semiconductor device which pastes these up with said adhesives, constitutes a layered roduct, is made to carry out the laminating of two or more these layered products where said semiconductor device arried in said wiring substrate is thoroughly held in said chip cavity section, and is characterized by providing the rocess which unifies these.

Claim 8] The process which forms two or more wiring substrates equipped with wiring formed in the principal plane, nd the process which makes the semiconductor device connected to said wiring and electric target carry in the wiring ubstrate equipped with said wiring, The process which forms two or more electric conduction beer insulating substrates vhich have the larger chip cavity section than the semiconductor device volume in which this semiconductor device is ıeld when said semiconductor device is carried, and formed the adhesives layer in the rear face, The laminating of two o nore of said electric conduction beer insulating substrate and said two or more wiring substrates is carried out by turns. The process which pastes these up with said adhesives, constitutes a layered product, is made to carry out the laminating f two or more these layered products where said semiconductor device carried in said wiring substrate is thoroughly ıeld in said chip cavity section, and unifies these, The manufacture approach of the semiconductor device characterized y providing the process which forms the beer which penetrates these where the laminating of said two or more layered roducts is carried out, and forms a connection electrode in this beer.

Claim 9] Make said two or more semiconductor devices carry in said wiring substrate, and said two or more chip cavity ections are formed in said electric conduction beer insulating substrate. The manufacture approach of the semiconductor levice according to claim 7 or 8 characterized by providing the process which cuts said unified layered product in the irection of a laminating after said unification process which carries out the laminating of two or more said layered roducts which carried out the laminating of said these wiring substrates and said electric conduction beer insulating ubstrate, and formed them, and is unified.

Claim 10] Said semiconductor device is the manufacture approach of the semiconductor device according to claim 7 to characterized by the thickness being abbreviation 30 thru/or 200 micrometers.

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: NOTICES *

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!.**** shows the word which can not be translated.
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)ETAILED DESCRIPTION

Detailed Description of the Invention]
0001]
Field of the Invention] This invention relates to the semiconductor device which used the laminating mold package vhich carries out the laminating of two or more semiconductor devices, and its manufacture approach.
0002]
Description of the Prior Art] For the purpose of high-density-assembly-izing, the laminating of the semiconductor levice is carried out and the semiconductor device uses it more often. The stacked package used conventionally is ndicated by JP,9-219490,A, JP,10-135267,A, and JP,10-163414,A. these conventional packages -- TSOP (Thin Small)utline Package), and TCP (Tape Carrier Package) and BAG (Ball Grid Array) etc. -- after assembling a package and naking it complete, by accumulating the external terminal beforehand prepared in each package according to an ndividual, the laminating of each is carried out and electrical installation is performed further. Namely, in addition, as 'or the conventional laminating mold package, the laminating processing process for every package is added like the ıssembler of each package. Therefore, it becomes the sequential method of construction which a routing counter ncreases by the laminating number, and the increase in cost by using members, such as a spacer which carries out a aminating according to the processing increase in cost by this method of construction and an individual, poses a big)roblem.
0003]
Problem(s) to be Solved by the Invention] moreover, the above-mentioned problem -- in addition, in the conventional :xample which is only the electrical installation section, in addition is indicated by JP,10-163414,A, JP,10-135267,A, :tc., since a semiconductor device is float structure, the mechanical strength of the package which repeats the package of ınother object and which boils rattlingly, and adhesion and a laminating interface produce for every package more, or :arried out the laminating has the problem that where of reservation of a mechanical strength is difficult and cannot .ecure sufficient dependability. Furthermore, for using for the medium it is [a medium] elastic like an IC card to form)y the conventional approach mentioned above to form the thin laminating mold package which fitted the thin .emiconductor chip whose thickness is 30 thru/or about 200 micrometers towards development of the semiconductor levice with which thin shape-ization progresses and application amplification of an IC card, a cellular phone, etc. will)rogress with densification from now on difficult, the problem was in applicability deficiently in resiliency. This nvention is made according to such a situation, is thinly excellent in sealing nature and resiliency, and offers the .emiconductor device using the laminating mold package which can be formed intricately and easily by the production)rocess, and its manufacture approach.
0004]
Means for Solving the Problem] Two or more wiring substrates equipped with wiring to which the semiconductor levice of this invention was electrically connected to two or more beer with which the connection electrode was formed, espectively, and this connection electrode, The semiconductor device which was carried in said wiring substrate and :onnected to said wiring and electric target, It has the larger chip cavity section than the semiconductor device volume in vhich this semiconductor device is held when said semiconductor device is carried. And two or more electric conductior)eer insulating substrates equipped with the connection electrode which embedded from two or more beer and was 'ormed are provided. One of said the electric conduction beer insulating substrates, and one of said the wiring substrates .o that said connection wiring of said electric conduction beer insulating substrate and said connection electrode of this viring substrate may be electrically connected to said wiring substrate A laminating is carried out and it is characterized 1st] by the laminating of two or more these layered products being carried out, and coming to unify them, where said .emiconductor device which constituted the layered product and was carried in said wiring substrate is thoroughly held n said chip cavity section.
0005] Moreover, two or more wiring substrates equipped with wiring to which the semiconductor device of this

nvention was electrically connected to two or more beer with which the connection electrode was formed, respectively, ınd this connection electrode, The semiconductor device which was carried in said wiring substrate and connected to ·aid wiring and electric target, Two or more electric conduction beer insulating substrates equipped with the connection :lectrode which has the larger chip cavity section than the semiconductor device volume in which this semiconductor levice is held when said semiconductor device is carried, embedded from two or more beer, and was formed, When the aminating of said wiring substrate and the electric conduction beer insulating substrate is carried out, a laminating is :arried out on the electric conduction beer insulating substrate of the maximum upper layer. The electric conduction beer nsulating substrate of the upper layer equipped with the connection electrode which embedded from two or more beer ınd was formed is provided. One of said the electric conduction beer insulating substrates and one of said the wiring ·ubstrates A laminating is carried out and a layered product is constituted so that said connection wiring of said electric :onduction beer insulating substrate and said connection electrode of this wiring substrate may be electrically connected o said wiring substrate. Where said semiconductor device carried in said wiring substrate is thoroughly held in said chip :avity section, this layered product is characterized [2nd] by the laminating of the more than one being carried out, and :oming to be unified. The thickness of said semiconductor device may be 30-200 micrometers of abbreviation.

0006] The laminating of said two or more layered products by which the laminating was carried out is carried out, and he lower layer electric conduction beer insulating substrate equipped with the connection electrode which embedded rom two or more beer and was formed is provided. The wiring substrate of a re-lower layer of said layered product is :ontacted in said 1st lower layer field of an electric conduction beer insulating substrate. Said connection electrode of ·aid wiring substrate of a re-lower layer and said connection electrode of said lower layer electric conduction beer nsulating substrate are connected electrically, and two or more external terminals electrically connected through the :onnection electrode and wiring which were formed in said beer may be made to be formed in said 2nd lower layer page 3etween said semiconductor devices contained by said chip cavity section and this chip cavity section of said electric :onduction beer insulating substrate, the space which absorbs stress may be made to be formed. Said space may be made o fill up with elasticity adhesives.

0007] By the above configurations, the semiconductor device which has a thin laminating mold package can be)btained. Moreover, since the upper and lower sides are inserted into the laminating mold package by the electric :onduction beer insulating substrate, the sealing nature to a semiconductor device is high. Moreover, although the ·emiconductor device is held in the chip cavity section currently formed in the electric conduction beer insulating ·ubstrate, since the thickness and area of the chip cavity section are smaller than a semiconductor device, even if a ·emiconductor device is held into this, space is formed between the semiconductor device and the wall of the chip cavity ·ection. For example, even if a semiconductor device is extended for a while by bending this semiconductor device, ·pace is between the chip cavity sections, and this space can absorb the elongation of a semiconductor device. Therefore, t becomes possible to absorb the stress generated even if external force joins a semiconductor device. Furthermore, ılthough this space will be filled up with the binder which joins an electric conduction beer insulating substrate and a viring substrate, if the binder of elasticity, such as silicon resin, is used especially, while absorption of stress is attained, ·ealing performance will improve and the moisture resistance of a semiconductor device will improve.

0008] The process which forms two or more wiring substrates with which the manufacture approach of the ·emiconductor device of this invention was equipped with wiring electrically connected to two or more beer with which he connection electrode was formed, respectively, and this connection electrode, The process which makes the ·emiconductor device connected to said wiring and electric target carry in said wiring substrate, It has the larger chip :avity section than the semiconductor device volume in which this semiconductor device is held when said ·emiconductor device is carried. Have the connection electrode which embedded from two or more beer and was formed ınd the process which forms two or more electric conduction beer insulating substrates in which the adhesives layer was ormed at the rear face is provided. One of said the electric conduction beer insulating substrates and one of said the viring substrates A laminating is carried out so that said connection wiring of said electric conduction beer insulating ·ubstrate and said connection electrode of this wiring substrate may be electrically connected to said wiring substrate. These are pasted up with said adhesives, a layered product is constituted, where said semiconductor device carried in ·aid wiring substrate is thoroughly held in said chip cavity section, the laminating of two or more these layered products s carried out, and it is characterized [1st] by providing the process which unifies these.

0009] Moreover, the process which forms two or more wiring substrates equipped with wiring with which the nanufacture approach of the semiconductor device of this invention was formed in the principal plane, The process vhich makes the semiconductor device connected to said wiring and electric target carry in said wiring substrate, The)rocess which forms two or more electric conduction beer insulating substrates which have the larger chip cavity section han the semiconductor device volume in which this semiconductor device is held when said semiconductor device is :arried, and formed the adhesives layer in the rear face, The laminating of two or more of said electric conduction beer nsulating substrate and said two or more wiring substrates is carried out by turns. The process with which said

emiconductor device which pasted these up with said adhesives, constituted the layered product, and was carried in said viring substrate carries out the laminating of two or more these layered products in the condition of having held in said :hip cavity section thoroughly, and unites these, It is characterized [2nd] by providing the process which forms the beer vhich these-penetrates said two or more layered products where a laminating is carried out, and forms a connection :lectrode in this beer. You may make it provide further the process which cuts said unified layered product in the lirection of a laminating after said unification process which carries out the laminating of two or more said layered)roducts which were made to carry said two or more semiconductor devices in said wiring substrate, formed said two or nore chip cavity sections in said electric conduction beer insulating substrate, carried out the laminating of said these viring substrates and said electric conduction beer insulating substrate, and formed them, and is unified. It becomes)ossible to manufacture by the routing counter smaller than the technique which carries out the laminating of the :onventional package by carrying out the laminating of a semiconductor device layer, the wiring substrate which upports this, and the electric conduction beer insulating substrate collectively, and cutting them.

0010]

Embodiment of the Invention] Hereafter, the gestalt of implementation of invention is explained with reference to a lrawing. First, with reference to drawing 1 , the semiconductor device using the laminating mold package which is the st example is explained. The perspective view of the semiconductor device with which the laminating mold package vas used for drawing 1 (a), and drawing 1 (b) are the perspective views showing the external terminal of the lower layer :lectric conduction beer laminate of a laminating mold package. Although this example is an example which carried out he laminating of the four semiconductor devices, in this invention, the number of the semiconductor devices which carry)ut a laminating is not limited to four pieces. The laminating of the two or more numbers to need can be carried out. The)ackage consists of lower layer electric conduction beer laminate 20b which has electric conduction beer laminate 20of :lectric conduction beer laminate [which holds a semiconductor device 5] 20, wiring substrate [in which a emiconductor device 5 is made to carry] 30, and the upper layer which seals package a, and the external terminal 10. That is, two or more layer laminating of the layered product of the electric conduction beer laminate 20 and the wiring ubstrate 30 is carried out between the upper layer and the lower layer electric conduction beer laminates 20a and 20b, ieating application of pressure is carried out and the package is constituted by one (refer to drawing 5).

0011] The electric insulating plates 6, such as a polyimide substrate with copper foil with a thickness of about 40 nicrometers or a print laminate, are used for the wiring substrate 30 in which a semiconductor device is carried. The :onnection electrode 7 (refer to drawing 4 (b)) is embedded by the electric insulating plate 6 from beer. The copper foil)n an electric insulating plate 6 is formed in the land 17 on the connection electrode 7, and other fields, and patterning is :arried out to the configuration which has the wiring 8 electrically connected with the semiconductor device 5. The hickness (thickness of a silicon chip) of a semiconductor device 5 is about 30-200 micrometers, and is about 50-150 nicrometers preferably. The electric insulating plates 1, such as a polyimide substrate with copper foil with a thickness)f about 75 micrometers or a print laminate, are used for the lead-wire beer laminate 20. The connection electrode 2 refer to drawing 4 (a)) is embedded by the electric insulating plate 1 from beer. Patterning of the copper foil on an :lectric insulating plate 1 is carried out to the configuration which has the land 3 on the connection electrode 2, and the viring 16 formed in other fields. The opening (chip cavity section) 12 which holds a semiconductor device is formed in a)art for the center section of an insulating substrate 1.

0012] In this invention, if the thickness of the electric conduction beer laminate 20 is the magnitude in which a emiconductor device 5 is held in opening 12, it may be the same thickness as the wiring substrate 30, or may be thin. Since the binder 4 is applied to the electric conduction beer laminate at this time, if unification processing is performed, he chip cavity section 12 will come to be filled up with adhesives 4. The upper electric conduction beer laminate 20a ha: viring and a land, and the connection electrode is embedded from beer. The land 3 is formed on the connection :lectrode. Moreover, lower layer electric conduction beer laminate 20b has wiring and a land, and the external terminal .0 is formed in the rear face.

0013] The semiconductor device of this example can obtain the semiconductor device which has a thin laminating mold)ackage by the above configurations. Moreover, since the upper and lower sides of a laminating are inserted by the :lectric conduction beer laminate, the sealing nature to a semiconductor device is high. Moreover, although the emiconductor device is held in the chip cavity section currently formed in the electric conduction beer laminate, since he thickness and area of the chip cavity section are smaller than a semiconductor device, even if a semiconductor device s held into this, space is formed between the semiconductor device and the wall of the chip cavity section. For example, :ven if a semiconductor device is extended for a while by bending this semiconductor device, space is between the chip :avity sections, and this space can absorb the elongation of a semiconductor device. Therefore, it becomes possible to ibsorb the stress generated even if external force joins a semiconductor device. Furthermore, although this space will be illed up with the binder of elasticity, such as an elastomer which joins the electric conduction beer laminate by which he laminating was carried out, and a wiring substrate, if the binder of elasticity, such as silicon resin, is used especially,

vhile absorption of stress is attained, sealing performance will improve and the moisture resistance of a semiconductor levice will improve.

0014] Next, the 2nd example is explained with reference to drawing 2 thru/or drawing 5 . Drawing 2 thru/or drawing 5 ıre the fragmentary sectional view of the semiconductor device shown in drawing 1 , and the production process ectional view of this semiconductor device, and is a production process sectional view explaining the manufacture ıpproach of a semiconductor device that the laminating of two or more semiconductor devices was carried out. This emiconductor device has realized the laminated structure of a semiconductor device by providing two or more electric onduction beer laminates 20 equipped with the opening 12 which has the space in which the semiconductor device 5 arried in two or more wiring substrates 30 with which a semiconductor device 5 is carried, and the wiring substrate 30 i: ıeld, and carrying out the laminating of the these electric conduction beer laminate 20 and the wiring substrate 30 by urns.

0015] The electric insulating plates 1, such as a polyimide substrate with copper foil or a print laminate, are used for the lectric conduction beer laminate 20. First, the electric insulating plates 1, such as a copper foil print laminate of a part vith which the beer on the electric insulating plates 1, such as a print laminate, and wiring are formed, form two or more eer 13 using an YAG laser, carbon dioxide gas laser, etc. Then, a mask 14 is given to the copper foil 15 of beer and a viring part, this is etched, and a circuit pattern 16 and a land 3 are formed. And from beer 13, the connection electrode 2 s embedded by screen-stenciling silver or the conductive resin paste containing a copper filler. To the formation ıpproach of the connection electrode 2, after performing coppering or gold plate to a beer wall, the approach of mbedding a conductive ingredient in beer is also possible. The heat-curing mold binders 4, such as an epoxy resin, are ıpplied to the rear face of the electric insulating plates 1, such as a print laminate. The field in which the semiconductor levice of the electric insulating plates 1, such as a print laminate, is held is pierced, and is used as the chip cavity section .2 (drawing 2).

0016] The electric insulating plates 6, such as a polyimide substrate with copper foil or a print laminate, are used for the viring substrate 30 in which a semiconductor device 5 is carried. The electric insulating plate 6 which consists of a opper foil print laminate of a part with which the beer on an electric insulating plate 6 and wiring are formed forms two r more beer using an YAG laser, carbon dioxide gas laser, etc. Then, a mask is given to the copper foil of beer and a viring part, this is etched, and a circuit pattern 8 and a land 17 are formed. And from beer, the connection electrode 7 is mbedded by screen-stenciling silver or the conductive resin paste containing a copper filler. To the formation approach f the connection electrode 7, after performing coppering or gold plate to a beer wall, the approach of embedding a onductive ingredient in beer is also possible. Die bond of the semiconductor device (chip) 5 is carried out to this wiring ubstrate 30 with a flip chip method of construction etc., and it is made to carry in it. In order to carry a semiconductor levice 5 in the wiring substrate 30, it comes to connect the connection terminals 11, such as a solder ball, with a circuit attern 8. The connection terminal 11 carries out coat protection with under-filling resin 9 (drawing 3). And a aminating is carried out so that the electric conduction beer laminate 20 may be aligned to this wiring substrate 30 and a emiconductor device 5 may be arranged at the chip cavity section 12 (drawing 4). Then, after aligning, a layered roduct is pressed with the curing temperature of a binder 4 with heating compressors, such as the vacuum press. Finally n accordance with each package appearance, a blade, a router, etc. cut, and a stacked package is formed (drawing 5).

0017] In this example, form two or more chip cavity sections in the electric conduction beer laminate 20, two or more emiconductor devices are made to carry in the wiring substrate 30, the laminating of these was carried out by turns, two r more semiconductor device layered products were formed, the blade was eventually carried out for every emiconductor device layered product, and the increase in efficiency of stacked package formation is calculated. In this xample, as shown in drawing 5 , for example, the four-piece laminating of the semiconductor device 5 is carried out, nd a layered product is constituted. It is inserted into the electric conduction beer laminates 20a and 20b with which the hip cavity section is not formed in the upper and lower sides of this layered product, and a semiconductor device 5 is ealed. The external terminal of a proper configuration is formed in lower layer electric conduction beer laminate 20b. It ecomes possible to manufacture by the routing counter smaller than the technique which carries out the laminating of he conventional package by carrying out the laminating of a semiconductor device layer, the wiring substrate which upports this, and the electric conduction beer insulating substrate collectively, and cutting them.

0018] Next, the 3rd example is explained with reference to drawing 6 and drawing 7 . Drawing 6 and drawing 7 are the roduction process sectional views explaining the manufacture approach of a semiconductor device that the laminating f two or more semiconductor devices was carried out. This semiconductor device has realized the laminated structure of semiconductor device by providing two or more electric conduction beer laminates 40 equipped with the opening 32 vhich has the space in which the semiconductor device 25 carried in two or more wiring substrates 50 with which a emiconductor device 25 is carried, and the wiring substrate 50 is held, and carrying out the laminating of the these lectric conduction beer laminate 40 and the wiring substrate 50 by turns. The electric insulating plates 21, such as a olyimide substrate with a copper thin layer or a print laminate, are used for the electric conduction beer laminate 40.

First, the copper foil print laminate 1 of a part with which the beer on the print laminate 1 and wiring are formed gives a nask to the copper foil of beer and a wiring part, etches this, and forms a land 23. The heat-curing mold binders 24, such is an epoxy resin, are applied to the rear face of the print laminate 1. The field in which the semiconductor device of the rint laminate 21 is held is pierced, and is used as the chip cavity section 32. In this example, it has the two chip cavity ections. In this invention, in order to calculate the increase in efficiency of a production process, it is advantageous to repare the two or more chip cavity sections in an electric conduction beer laminate.

0019] The electric insulating plates 26, such as a polyimide substrate with a copper thin layer or a print laminate, are sed for the wiring substrate 30 in which a semiconductor device 25 is carried. A mask is given to the beer of the print aminate 26, and the copper foil of a wiring part, this is etched, and a circuit pattern 28 and a land 37 are formed. Die ond of the semiconductor device (chip) 25 is carried out to this wiring substrate 50 with a flip chip method of onstruction etc., and it is made to carry in it. In this example, two semiconductor devices 25 are carried in the wiring ubstrate 50. And a laminating is carried out so that the electric conduction beer laminate 40 may be aligned to this viring substrate 50 and a semiconductor device 25 may be arranged at the chip cavity section 32. Then, after aligning, a ayered product is pressed with the curing temperature of a binder 24 with heating compressors, such as the vacuum ress. Since a binder 24 is stiffened, the through hole 33 which uses an about 0.4mm drill for the lands 23 and 37 which orm beer from the aperture of 0.25mm, and penetrates these lands is formed. After that, on the interior of a through hole 3, and a land, electroplating, such as copper and gold, is performed and the connection electrode 31 is formed. Finally n accordance with each package appearance, a blade, a router, etc. cut, and a stacked package is formed.

0020] In this example, form two or more chip cavity sections in the electric conduction beer laminate 40, two or more emiconductor devices are made to carry in the wiring substrate 50, the laminating of these was carried out by turns, two r more semiconductor device layered products were formed, the blade was eventually carried out for every emiconductor device layered product, and the increase in efficiency of stacked package formation is calculated. In this xample, for example, the four-piece laminating of the semiconductor device 25 is carried out, and a layered product is onstituted. It is inserted into the electric conduction beer laminates 40a and 40b with which the chip cavity section is no ormed in the upper and lower sides of this layered product, and a semiconductor device 25 is sealed. The external erminal of a proper configuration is formed in the rear face at lower layer electric conduction beer laminate 40b. It ecomes possible to manufacture by the routing counter smaller than the technique which carries out the laminating of he conventional package by carrying out the laminating of a semiconductor device layer, the wiring substrate which upports this, and the electric conduction beer insulating substrate collectively, and cutting them.

0021] Next, the 4th example is explained with reference to drawing 8 . Drawing 8 is the sectional view of a emiconductor device. In this example, it has processed to the same semiconductor device as the 3rd example shown in lrawing 7 . This semiconductor device has realized the laminated structure of a semiconductor device by providing two r more wiring substrates 50 with which a semiconductor device 25 is carried, and two or more electric conduction beer aminates 40 equipped with the space in which the semiconductor device 25 carried in the wiring substrate 50 is held, nd the chip cavity section 32, and carrying out the laminating of the these electric conduction beer laminate 40 and the viring substrate 50 by turns. For example, the four-piece laminating of the semiconductor device 25 is carried out, and a ayered product consists of this example. It is inserted into the electric conduction beer laminates 40a and 40b with whicl he chip cavity section is not formed in the upper and lower sides of this layered product, and a semiconductor device 25 s sealed.

0022] The connection electrode 31 connected to each semiconductor device 25 through wiring at this layered product is ormed in the interior of the beer of a layered product. The path cord 31 consists of connection electrodes 31b and 31c onnected with connection electrode 31a connected with a grand (GND) line, and a signal line. Furthermore, the metal nembranes 33, such as aluminum and copper, are formed in the upper layer and the lower layer electric conduction beer aminates 40a and 40b. A metal membrane is formed for example, by the sputtering method, or is formed from a metallic oil. It connects with connection electrode 31a connected with a grand line electrically, and this metal membrane 33 is in condition non-contact in the connection electrodes 31b and 31c connected with a signal line. A metal membrane 33 omes to have a shielding effect by connecting with a grand line. This effectiveness can be adjusted by adjusting suitably n ingredient, width of face, etc. of the ingredient of a metal membrane, or a thickness and a connection electrode.

0023] Next, the 5th example is explained with reference to drawing 9 . Drawing 9 is the sectional view of the emiconductor device included in a semiconductor device and this semiconductor device. In this example, it has rocessed to the same semiconductor device as the 3rd example shown in drawing 7 . This semiconductor device has ealized the laminated structure of a semiconductor device by providing two or more wiring substrates 50 with which a emiconductor device 25 is carried, and two or more electric conduction beer laminates 40 equipped with the space in vhich the semiconductor device 25 carried in the wiring substrate 50 is held, and the chip cavity section 32, and carrying ut the laminating of the these electric conduction beer laminate 40 and the wiring substrate 50 by turns. For example, he four-piece laminating of the semiconductor device 25 is carried out, and a layered product consists of this example. It

s inserted into the electric conduction beer laminates 40a and 40b with which the chip cavity section is not formed in the ıpper and lower sides of this layered product, and a semiconductor device 25 is sealed. Through the bump 34 who is the :onnection electrode which attached silicon chips a, b, C, and D in each, the laminating of the semiconductor device 25 ısed for this semiconductor device is carried out one by one, and it is constituted. In this example, a stacked package nore possible [making it a multilayer further] than the semiconductor device of the 1st thru/or the 4th example and thin noreover can be obtained.

0024]

Effect of the Invention] This invention can obtain the semiconductor device which has a thin laminating mold package ›y the above configuration. Moreover, since the upper and lower sides are inserted into the laminating mold package by he electric conduction beer insulating substrate, it can make sealing nature to a semiconductor device high. Moreover, ılthough the semiconductor device is held in the chip cavity section currently formed in the electric conduction beer nsulating substrate, since the thickness and area of the chip cavity section are smaller than a semiconductor device, even f a semiconductor device is held into this, space is formed between the semiconductor device and the wall of the chip :avity section. Therefore, it becomes possible to absorb the stress generated even if external force joins a semiconductor levice. Furthermore, when this space is filled up with the binder which joins an electric conduction beer insulating ubstrate and a wiring substrate and the binder of elasticity, such as silicon resin, is used especially, while absorption of tress is attained, sealing performance improves and the moisture resistance of a semiconductor device improves. Moreover, it becomes possible to manufacture by the routing counter smaller than the technique which carries out the aminating of the conventional package by carrying out the laminating of a semiconductor device layer, the wiring ubstrate which supports this, and the electric conduction beer insulating substrate collectively, and cutting them.

Translation done.]